CLAIMS

What is claimed is:

1. A method for controlling programming voltage levels of non-volatile memory cells, the method comprising:

providing a resistive divider connected to a programming voltage reference and effective to generate at least one programming voltage level;

providing a reference cell crossed by a cell current; and

wherein cell current is applied to the resistive divider to correlate the programming voltage level to intrinsic features of the reference cell.

2. A control method according to claim 1 wherein the cell current is applied to the resistive divider in shunt configuration.

3. A control method according to claim 2 wherein the cell current is applied to an end of a resistive element comprised in the resistive divider and having a further end connected to the programming voltage reference.

4. A control method according to claim 1 wherein the reference cell is identical to the non-volatile memory cells to be programmed.

5. A control method according to claim 1, further comprising generating the programming voltage level with a high, respectively low, value for a low, respectively high, value of the cell current.

6. A control method according to claim 1, further comprising the resistive divider generating a plurality of programming voltage levels, wherein the programming voltage levels are obtained with a centering and separation correlated to intrinsic features of the non-volatile memory cells to be programmed.

7. A control method according to claim 5 wherein the voltage levels are moved closer, respectively away, in the case of fast, respectively slow, memory cells to be programmed.

8. A control method according to claim 5 wherein the voltage levels have reciprocal distances being lower, respectively higher, in the case of fast, respectively slow, non-volatile memory cells to be programmed.

9. A control method according to claim 1, further comprising providing a feedback of a current flowing in the resistive divider to correlate the programming voltage level to variations of the programming voltage reference.

10. A control method according to claim 1 wherein the feedback increases, respectively decreases, the cell current value applied to the divider in case of decrease, respectively increase, of the programming voltage reference.

11. A programming voltage regulator of non-volatile memory cells comprising at least an input stage inserted between a first and a second voltage reference and connected to a reference memory cell, as well as, in correspondence with an output terminal of the input stage, to a resistive divider, in turn inserted between a programming voltage reference and the second voltage reference and connected to at least an output terminal of the regulator, effective to supply a programming voltage to the non-volatile memory cells, wherein the output terminal of the input stage is connected to a first circuit node of the resistive divider in correspondence with an end of a resistive element included in the resistive divider and having a further end connected to the programming voltage reference, a voltage value on the first circuit node being thus obtained by shunting the programming voltage reference.

12. A voltage regulator according to claim 11 wherein the reference memory cell is identical to the non-volatile memory cells to be programmed.

13. A voltage regulator according to claim 11 wherein the reference memory cell has a control terminal connected to a band-gap voltage reference.

14. A voltage regulator according to claim 11 wherein the reference memory cell has a control terminal connected to a self-biasing network inserted between the first and second voltage reference and including a first transistor inserted between the first and second voltage reference and having a control terminal connected to a second circuit node, a second transistor inserted between the control terminal of the reference memory cell and the second voltage reference and a third transistor connected to the second voltage reference and to the output terminal of the input stage, the second and third transistor having control terminals connected to each other and to the second circuit node.

15. A voltage regulator according to claim 14 wherein the self-biasing network further comprises a capacitor inserted in parallel to the second transistor between the control terminal of the reference memory cell and the second voltage reference.

16. A voltage regulator according to claim 15 wherein the self-biasing network further comprises a fourth transistor inserted between the first voltage reference and the control terminal of the reference memory cell and having a control terminal connected to the second circuit node.

17. A voltage regulator according to claim 15 wherein the self-biasing network further comprises a fourth transistor inserted between the output terminal of the

input stage and the control terminal of the reference memory cell and having a control terminal connected to the second circuit node.

18. A voltage regulator according to claim 11 wherein the input stage comprises a cascode block inserted between a biasing block and the reference memory cell, the biasing block comprising a first transistor being diode-connected and inserted between the first voltage reference and the cascode block, and a second transistor connected to the first voltage reference and having a control terminal connected to a control terminal of the first transistor.

19. A voltage regulator according to claim 18 wherein the cascode block comprises a cascode transistor inserted between the biasing block and the reference memory cell and having a control terminal connected through a buffer to the reference memory cell.

20. A voltage regulator according to claim 18 wherein the cascode block comprises a cascode transistor inserted between the biasing block and the reference memory cell and having a control terminal connected to a third circuit node of a second resistive divider included in a self-biasing network.

21. A voltage regulator according to claim 20 wherein the second resistive divider is inserted between a second circuit node and a third transistor of the self-biasing network and includes a first and a second resistive element interconnected in correspondence with the third circuit node.

22. A voltage regulator according to claim 11, further comprising an output stage inserted between the programming voltage reference and the output terminal of the regulator and connected to the first circuit node of the resistive divider, the output stage including an amplifier powered by the programming voltage reference

and having a first input terminal connected to the first circuit node and a second input terminal connected to the output terminal, as well as a transistor inserted between the programming voltage reference and the output terminal and having a control terminal connected to an output terminal of the amplifier.

23. A programming voltage regulator of non-volatile multilevel memory cells comprising at least an input stage inserted between a first and a second voltage reference and connected to a reference memory cell, as well as, in correspondence with an output terminal of the input stage, to a resistive divider, in turn inserted between a programming voltage reference and the second voltage reference and having a plurality of circuit nodes connected to a plurality of output terminals of the regulator, effective to supply a plurality of programming voltage values for different levels of multilevel non-volatile memory cells, wherein the output terminal of the input stage is connected to a first circuit node of the resistive divider in correspondence with an end of a resistive element included in the resistive divider and having a further end connected to the programming voltage reference, a voltage value on the first circuit node being thus obtained by shunting the programming voltage reference.

24. A voltage regulator according to claim 23, further comprising a plurality of output stages, input-connected to the plurality of circuit nodes of the resistive divider, as well as to a plurality of output terminals to provide the plurality of programming voltage values for different levels of multilevel non-volatile memory cells.

25. A voltage regulator according to claim 23 wherein the reference memory cell is identical to the non-volatile memory cells to be programmed.

26. A voltage regulator according to claim 23 wherein the reference memory cell has a control terminal connected to a band-gap voltage reference.

27. A voltage regulator according to claim 23 wherein the reference memory cell has a control terminal connected to a self-biasing network inserted between the first and second voltage reference and including a first transistor inserted between the first and second voltage reference and having a control terminal connected to a second circuit node, a second transistor inserted between the control terminal of the reference memory cell and the second voltage reference and a third transistor connected to the second voltage reference and to the output terminal of the input stage, the second and third transistor having control terminals connected to each other and to the second circuit node.

28. A voltage regulator according to claim 27 wherein the self-biasing network further comprises a capacitor inserted in parallel to the second transistor between the control terminal of the reference memory cell and the second voltage reference.

29. A voltage regulator according to claim 28 wherein the self-biasing network further comprises a fourth transistor inserted between the first voltage reference and the control terminal of the reference memory cell and having a control terminal connected to the second circuit node.

30. A voltage regulator according to claim 28 wherein the self-biasing network further comprises a fourth transistor inserted between the output terminal of the input stage and the control terminal of the reference memory cell and having a control terminal connected to the second circuit node.

31. A voltage regulator according to claim 23 wherein the input stage comprises a cascode block inserted between a biasing block and the reference memory cell, the biasing block comprising a first transistor being diode-connected and inserted between the first voltage reference and the cascode block, and a second transistor

connected to the first voltage reference and having a control terminal connected to a control terminal of the first transistor.

32. A voltage regulator according to claim 31 wherein the cascode block comprises a cascode transistor inserted between the biasing block and the reference memory cell and having a control terminal connected through a buffer to the reference memory cell.

33. A voltage regulator according to claim 31 wherein the cascode block comprises a cascode transistor inserted between the biasing block and the reference memory cell and having a control terminal connected to a third circuit node of a second resistive divider included in a self-biasing network.

34. A voltage regulator according to claim 33 wherein the second resistive divider is inserted between a second circuit node and a third transistor of the self-biasing network and includes a first and a second resistive element interconnected in correspondence with the third circuit node.

35. An apparatus to control programming voltage levels of non-volatile memory cells, the apparatus comprising:

a reference cell to generate a cell current representative of intrinsic features of the reference cell;

a circuit block having an input terminal coupled to the reference cell to receive the cell current and having an output terminal to provide an output voltage that can change in response to a change in the cell current; and

a resistive divider, coupled to the output terminal of the circuit block, to receive the output voltage and to generate at least one programming voltage level value therefrom that is correlated to the intrinsic features of the reference cell.

36. The apparatus of claim 35 wherein the output voltage provided by the circuit block is a shunt of a programming voltage reference.

37. The apparatus of claim 37 wherein the circuit block includes:

a biasing block;

a cascode block coupled between the biasing block and the reference cell; and

a self-biasing network coupled to the biasing block and to the resistive divider.

38. The apparatus of claim 1 wherein the resistive divider includes a plurality of nodes, each of the plurality of nodes being coupled to respectively provide a different programming voltage level value for different levels of the non-volatile memory cells.

39. A system for controlling programming voltage levels of non-volatile memory cells, the system comprising:

a means for providing a cell current representative of intrinsic features of a reference cell;

a means for applying the cell current to a resistive divider; and

a means for generating at least one programming voltage level value from the resistive divider based on the applied cell current, the programming voltage level value being responsive to a change in the cell current and being correlated to the intrinsic features of the reference cell.

40. The system of claim 39 wherein the means for applying the cell current to the resistive divider includes at least one of a bias network, cascode network, and self-biasing network.